THIS OPINION WAS NOT WRITTEN FOR PUBLICATION

The opinion in support of the decision being entered today (1) was not written for publication in a law journal and (2) is not binding precedent of the Board.

Paper No. 15

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte JAMES D. BEASOM

Appeal No. 96-1584
Application No. 08/066,697[1]

ON BRIEF

Before URYNOWICZ, KRASS, and FLEMING, Administrative Patent Judges.

URYNOWICZ, Administrative Patent Judge.

DECISION ON APPEAL

This appeal is from the final rejection of claims 2-9, 11-18 and 20-24, all the claims pending in the application.

The invention pertains to semiconductor devices and is directed to the biasing of support material surrounding a

[1] Application for patent filed May 24, 1993. According to the appellant, the Application is a continuation of 07/827,095, filed January 27, 1992, now abandoned.

dielectrically isolated island, such as the fill material of a trench isolated integrated circuit architecture, so as to prevent the avalanche-generation of electron/hole pairs at a buried layer/island junction, which would otherwise limit the breakdown voltage of the device.

Claims 22 and 24 are illustrative and read as follows:

22. A semiconductor device comprising:

a semiconductor substrate containing a semiconductor island region of a first conductivity type having sidewalls which abut a first side of dielectric material that prescribes said island region, a second side of said dielectric material being contiguous with material capable of distributing a voltage applied thereto;

a first semiconductor region of said first conductivity type, and having an impurity concentration different from that of said island region, disposed in said island region, so as to define a relatively high-to-low impurity concentration junction between said first semiconductor region and said island region, said relatively high-to-low impurity concentration junction corresponding to a readily measurable transition of doping concentration within said island region, as opposed to a graded profile from high-to-low doping such as a Gaussian distribution from a top surface of said island region toward the bottom of said island region or a low-to-high retrograde profile measured from said top surface of said island region, said relatively high-to-low impurity concentration junction intersecting said dielectric material at a sidewall of said semiconductor island region;

a second semiconductor region of a second conductivity type disposed in said island region so as to define a PN junction between said second semiconductor region and said island region, said island region and said second semiconductor region being coupled to receive respective bias voltages which reverse bias said PN junction; and

wherein said PN junction is spaced apart from said sidewalls of said semiconductor island region, and said material capable of distributing a voltage applied thereto is coupled to receive a prescribed bias voltage that is insufficient to cause the avalanche-generation of electron-hole pairs in the vicinity of said relatively high-to-low impurity concentration junction.

24. A semiconductor device comprising:

a semiconductor substrate containing a semiconductor island region of a first conductivity type having sidewalls which abut a first side of dielectric material that prescribes said island region, a second side of said dielectric material being contiguous with material capable of distributing a voltage applied thereto;

a first semiconductor region of said first conductivity type, and having an impurity concentration different from that of said island region, disposed in said island region and defining a relatively high-to-low impurity concentration junction between said semiconductor region and said island region, said relatively high-to-low impurity concentration junction intersecting said dielectric material at a sidewall of said semiconductor island region, said relatively high-to-low impurity concentration junction corresponding to a readily measurable transition of doping concentration within said island region, as opposed to a graded profile from high-to-low doping such as a Gaussian distribution from a top surface of said island region toward the bottom of said island region or a low-to-high retrograde profile measured from said top surface of said island region;

a second semiconductor region of a second conductivity type disposed in said island region and defining a PN junction between said second semiconductor region and said island region, said island region and said second semiconductor region being coupled to receive respective bias voltages which reverse bias said PN junction; and

wherein said PN junction is spaced apart from said sidewalls of said semiconductor island region, and said material capable of distributing a voltage applied thereto is coupled to receive a prescribed bias voltage, said prescribed bias voltage having a value such that, when said material capable of distributing a voltage applied thereto is biased at said prescribed bias

voltage, said PN junction has a breakdown voltage which is greater than the breakdown voltage of said PN junction when said material capable of distributing a voltage applied thereto is biased at the same bias voltage applied to said second semiconductor region.

The references relied upon by the examiner as evidence of anticipation and obviousness are:

Taylor	4,231,056	Oct. 28, 1980
Muramatsu	4,470,062	Sep. 4, 1984
Piotrowski	4,665,425	May 12, 1987

The appealed claims stand rejected as follows:

a) claims 4-6, 8, 9, 13-15, 17, 18 and 22-24 are rejected under 35 U.S.C. § 103 as being unpatentable over Muramatsu in view of Piotrowski.

b) claims 2, 3, 7, 11, 12, 16 and 21 are rejected under 35 U.S.C. § 103 as being unpatentable over Muramatsu and Piotrowski, further in view of Taylor.

The final rejection (Paper No. 8) fails to treat claim 20. In its appeal brief, appellant has inferred that claim 20 would have been included in the group of claims identified above as b) and rejected under 35 U.S.C. § 103 over Muramatsu, Piotrowski and Taylor on pages 3 and 4 of the final rejection. For purposes of this appeal, like appellant, we will treat claim 20 along with claim 21, which depends from claim 20.

The respective positions of the examiner and the appellant with regard to the propriety of these rejections are set forth in the final rejection (Paper No. 8) and the examiner's answer (Paper No. 12) and the appellant's brief (Paper No. 11).

APPELLANT'S INVENTION

In FIG. 1 appellant discloses an integrated circuit architecture wherein substrate 13 is coupled to receive a bias V_b, the value of which is the same or close to the voltage applied to the N- island 11. As a result, the voltage differential across dielectric layer 15 is effectively zero so that no electron/hole pairs will be induced at interface 27 between N- region 11 and region 25. This limitation on the voltage differential between the island and substrate ensures that the electric field generated as a result of the substrate bias voltage is never high enough to cause avalanche generation of electron/hole pairs at interface 27 so as to degrade the breakdown voltage characteristic of the device at the PN junction 31.

FIGS. 2 and 3 are examples of trench-isolated island integrated circuit architectures. In order to prevent hole/electron pairs from being generated at the N-/N+ island/buried layer interface 27, which would degrade the

breakdown voltage characteristic of the device at PN junction 31, the bias voltage V_b is set at a value which is the same as or close to the voltage applied to the island 11. The bias voltage can differ from the island voltage by a value no more than half the total voltage applied to the integrated circuit.

THE PRIOR ART

In FIG. 2, Muramatsu discloses a sectional view of the semiconductor device illustrated in FIG. 1. N- island region 12A is formed on a P type semiconductor substrate 10. These elements correspond to appellant's island region 11 and substrate 13 in FIG. 3. N+ buried region 11A, corresponding to appellant's N+ region 25, is formed between region 12A and substrate 10. Muramatsu's film 18a formed on the surface of isolation groove 19 corresponds to appellant's film 43 on the surface of its groove, the polycrystalline insulation layer 20 in groove 19 corresponds to appellant's trench fill material 45 and P type region 13 corresponds to appellant's P type region 33.

In FIG. 5g, Muramatsu discloses that the N+ buried region 33A and P-type region 31 corresponding to elements 11A and 13 of FIG. 2, respectively, can be connected to the sidewalls of the trench at insulation layer 18''.

In FIG. 9, Piotrowski discloses a semiconductor structure having an NPN transistor having an N/N+ junction intersecting an island insulating layer and a P-type region spaced from the layer.

Taylor discloses a semiconductor RAM cell having a common contact region 23 connecting a trench 32 with the N- island region 22.

THE REJECTIONS UNDER 35 U.S.C. § 103

In its brief at page 12, appellant indicates that independent claim 23 stands or falls with independent claim 22 and at page 21, appellant indicates that claims 4-6, 8 and 9 stand or fall with the rejection of claim 22, from which they depend, and that claims 13-15, 17 and 18 stand or fall with the rejection of claim 23, upon which they depend. At page 26 of the brief, appellant further indicates that the Board's decision on the patentability of claims 11, 12 and 16, which depend from claim 23, stands or falls with the decision on patentability of claims 2, 3 and 7, respectively, which claims depend from claim 22. Lastly, at page 26 of the brief, appellant indicates that, whereas dependent claims 20 and 21 further delimit claim 24 in the same manner that claims 2 and 3 further delimit claim 22, the

rejection of claims 20 and 21 stands or falls with the rejection of claims 2 and 3, as applied to claim 24.

CLAIMS 22, 23, 4-6, 8, 9, 13-15, 17 and 18

After consideration of the positions and arguments presented by both the examiner and the appellants, we have concluded that the rejection of claims 22, 23, 4-6, 8, 9, 13-15, 17 and 18 should be sustained. We agree in general with the comments made by the examiner; we add the following discussion for emphasis.

With respect to claim 22, appellant asserts to the effect that the claim requires that the PN junction in the island region be spaced apart from the sidewalls of the island region whereat the dielectric material is formed, on the one hand, and that the high-to-low impurity concentration junction intersect the sidewalls of the island region and notes that neither embodiment of Muramatsu relied on by the examiner, FIGS. 2 and 5g, includes these two features. Still further, appellant argues to the effect that Muramatsu does not specifically teach that its trench material 20 is coupled to receive a bias voltage that is insufficient to cause the avalanche-generation of electron-hole pairs in the vicinity of the relatively high-to-low impurity concentration junction.

We are of the opinion that the subject matter of claim 22, and thus that of claims 23, 4-6, 8, 9, 13-15, 17 and 18, would have been obvious to one of ordinary skill in the art at the time the invention was made. As noted by the examiner, in FIG. 9, which is analogous to appellant's FIG. 1, Piotrowski shows a high-to-low impurity concentration junction intersecting an insulating material at the sidewalls of the semiconductor island region and a PN junction below contact 156 in the island region spaced apart from the sidewalls. To extend the corresponding junction to the sidewalls in the embodiment of FIG. 2 of Muramatsu or, in the alternative, to space the PN junction formed at P-type region 31 from the sidewalls of the semiconductor island region would have been obvious in view of the aforementioned teachings of Piotrowski. The suggestion to combine the teachings of the references flows from the fact that each concerns semiconductor structure having surface island regions formed by isolation walls. Appellant does not assert unexpected results from extending the aforementioned junction of Muramatsu's FIG. 2 embodiment or spacing region 31 of the reference's FIG. 5g embodiment or even argue against the obviousness of combining Muramatsu and Piotrowski with respect to this subject matter. Appellant merely states to the effect that

neither reference alone discloses the claimed structure. Results obtained from appellant's specific construction appear to be nothing more than those which would have been expected by the artisan. Expected results are evidence of obviousness. In re Skoner, 517 F.2d 947, 950, 186 USPQ 80, 82 (CCPA 1975).

The fact that Muramatsu does not state that voltage on its trench material 20 during device operation is insufficient to cause the avalanche-generation in question is not deemed controlling here. There is no disclosure in Muramatsu that its apparatus suffers from such degradation nor has appellant submitted any evidence to establish that as a fact. Appellant acknowledges at page 3, lines 16-22, of its specification that avalanche-generation of electron/hole pairs occurs only under certain conditions, such as when the amount of voltage applied to the device substrate is of sufficient magnitude to produce a strong electric field.

CLAIMS 2, 3, 7, 11, 12 and 16

We are of the opinion that the rejection of these claims under 35 U.S.C. § 103 as obvious over Muramatsu, Piotrowski and Taylor cannot be sustained and we will reverse the rejection.

The examiner observes that Taylor, unlike Muramatsu who grounds trench material 20, provides a common electrode 23 connecting trench material 32 and island region 22. According to the examiner,

> It would have been obvious to a skilled artisan to combine the teachings of Taylor as to how to apply voltages to the isolation structure with the analogous structure of Muramatsu and Piotrowski in order to insure full isolation of the semiconductor devices. (Answer, p. 4, last paragraph)

With respect to dependent claims 2 and 3, which in effect set forth a range for the prescribed bias voltage, the examiner has set forth no argument in support of the rejection. As to dependent claim 7, electrode 23 of Taylor is provided to interconnect trench resistor 32 and island collector region 22 of transistor Q_2, not to insure full isolation of semiconductor devices. There appears to be no motivation for combining Taylor's interconnect of circuit elements with Muramatsu and Piotrowski.

CLAIMS 20, 21, and 24

Independent claim 24 recites,

> said prescribed bias voltage having a value such that, when said material capable of distributing a voltage applied thereto is biased at said prescribed bias voltage, said PN junction has a breakdown voltage which is greater than the breakdown voltage of said PN junction when said material capable of distributing a voltage applied thereto is biased at the same bias voltage applied to said second semiconductor region.

Neither Muramatsu nor Piotrowski recognize the potential breakdown voltage problem addressed by appellant, nor his solution of applying a prescribed bias voltage to the material capable of distributing a voltage, the trench material 45, to prevent deterioration of the breakdown voltage at the PN junction 31. Accordingly, we shall not sustain the rejection of independent claim 24 or claims 20 and 21 which depend therefrom.

SUMMARY

In summary:

a) the decision of the examiner to reject claims 4-6, 8, 9, 13-15, 17, 18, 22 and 23 is affirmed.

b) the decision of the examiner to reject claims 2, 3, 7, 11, 12, 16, 20, 21 and 24 is reversed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 CFR § 1.136(a).

AFFIRMED-IN-PART

STANLEY M. URYNOWICZ, Jr. Administrative Patent Judge	)
ERROL A. KRASS Administrative Patent Judge	) BOARD OF PATENT APPEALS AND INTERFERENCES
MICHAEL R. FLEMING Administrative Patent Judge	)

Appeal No. 96-1584
Application 08/066,697

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APPEAL NO. 96-1584 - JUDGE URYNOWICZ
APPLICATION NO. 08/066,697

APJ URYNOWICZ

APJ FLEMING

APJ KRASS

DECISION: **AFFIRMED-IN-PART**

Typed By: Jenine Gillis

DRAFT TYPED: 27 Nov 98

FINAL TYPED: